Mrs. J.Dhurga Devi
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Present Position

Assistant Professor, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai from December-2007.

Present Additional Responsibility

- Deputy Director, Centre for Academic Courses, Anna University, Chennai from September-2018.

Previous Positions

- Lecturer, Department of Electronics and Communication Engineering, College of Engineering Guindy, Anna University, Chennai during March-2005 and December-2007.

Previous Additional Responsibility

- Phd Coordinator, Department of Electronics and Communication Engineering, Anna University, Chennai during January-2008 and November-2014.
- Student Counsellor, , Anna University, Chennai.

Other Employment

- Lecturer, Sri Manakula Vinayagar College of Engineering, Pondicherry for 3years.
- Lecturer, Amrita Institute of Technology for 1year and 4 months.

Degree

- M.E. in Communication Systems, Mepco Schlenk College of Engineering, Madurai Kamraj Unversity (1999 - 2000).
- B.E. in ELECTRONICS AND COMMUNICATION ENGG , Periyar Maniammai College of Technology for Women, Barathidasan University (1996 - 1999).

Research Degree

- Ph.D. in VLSI from Faculty of Information and Communication, College of Engineering, Anna University (2006 - 2014).
  Title: Investigations on Performance Improvements of Self Biased Adaptive Bandwidth PLL.

Area of Specialisation

- VLSI, Communication Sytems

Research Guidance

Number of Ph.D Scholars Guiding : 1
Number of M.E./ M.Tech. Projects Guided : 14
Number of M.E./ M.Tech. Projects Guiding : 3

Papers Published in Journals

Research Papers Published in International Journals : 4
Research Papers Published in National Journals : 0

1. Khalil I. Mahmoud, R. Rajasekar, J. Dhurga Devi, P.V. Ramakrishna, "Studies on Sensitivity of Clock and Data Recovery Circuits to Power Supply Noise", International Journal of Design, Analysis and Tools for Circuits And Systems, Vol. 1, Issue 1, pp. 16-21 (2011).

2. "Design of Delay Interpolator based Differental Self biased PLL", Journal of theoretical and Applied Information Technology, Vol. 58, Issue 3, pp. 582-588. (2013).

3. J.Dhurga Devi, " Jitter Reduced Self Biased PLLs—A Systematic Simulation Study", Circuits and Systems, published by Scientific Research. Vol. 7, Issue 6, pp. 533-542 (2016).

4. Vinodhini Gunasekaran ; Boby George ; Sankaran Aniruddhan ; Dhurga Devi Janardhanan ; Ramakrishna Venkatraman Palur, "Performance Analysis of Oscillator Based Read-out Circuit for LVDT", IEEE Transactions on Instrumentation and Measurement , published by IEEE . pp. 1-9 (2018).

Papers Presented in Programmes

Research Papers Presented in International Programmes : 4
Research Papers Presented in National Programmes : 0

1. Khalil Ibrahim Mahmoud, Dhurga Devi, J& Ramakrishna, "Design and Analysis of a Dual Loop CDR using Maneatis Delay Cell VCO" presented in a International level conference on The Fourth International Conference on Advances in Circuits, Electronics and Micro-electronics (CENICS 2011), French Riviera, France., France .

2. Deepan.E, Devi, J.D. ; Ramakrishna, P.V., "Performance improvement for Maneatis PLL for Microprocessor Clock" presented in a International level conference on 7th International conference on Ph.D Research In Microelectronics and Electronics, Trento, Italy., Italy .

3. "Design of C-band frequency synthesizer for FMCW transmitter " presented in a International level conference on International Conference on Circuits, Communication, Control and Computing, India .

4. "A CMOS Instrumentation Amplifier Using gm/ID Methodology for Sensor Readout Systems" presented in a International level conference on International Conference on Circuits, Communication, Control and Computing.

Current Sponsored Projects

1. "Development of Anusat-2" (September-2013 - November-2018). Project Cost: 24.00.

Sponsored Projects Completed

1. "Design OfPsuedo-Random Code Based Systems forRanging And Communication Applications", funded by Research Centre Imarat (RCI), DRDO, Hyderabad (January-2011 - January-2012). Project Cost: 9.70.

2. "Hardware System Design for Nondestructive Testing", funded by Lucid Software Design Systems, Inc, Chennai (September-2014 - March-2015). Project Cost: 4.00.

Programme Chaired

1. level .

Programme Attended

1. Participated in a International level workshop on "Intellisence Workshop and User onference" organized by IntelliSense Corp, USA and Bigtec PVT. Ltd., Bangalore, INDIA from 07-Aug-2006 to 08-Aug-2006.

2. Participated in a International level conference on "20th international conference on VLSI design" organized by VLSI Society of India, INDIA from 06-Jan-2007 to 10-Jan-2007.

3. Participated in a International level workshop on "2nd workshop on Mixed-Signal VLSI Design and Test" organized by VLSI Society of India, INDIA from 25-Apr-2007 to 26-Apr-2007.

4. Participated in a National level workshop on "workshop on Mentoring youth and adolescents" organized by CEG, Anna University, INDIA from 17-May-2007.

5. Participated in a International level conference on "24th international conference on VLSI design" organized by VLSI Society of India, INDIA from 04-Jan-2008 to 06-Jan-2008.

6. Participated in a International level conference on "21st international conference on VLSI design" organized by VLSI Society of India, INDIA from 04-Jan-2008 to 06-Jan-2008.

7. Attended a International level Short Course on "Advanced Analog IC design" organized by NIT Trichy, INDIA from 24-Sep-2008 to 25-Sep-2008.

8. Attended a International level Short Course on "AICTE QIP Shart term course on Recent developments in Network Security" organized by CEG, Anna University, INDIA from 02-Mar-2009 to 15-Mar-2009.

9. Attended a International level Short Course on "FDP on EC2305- Transmission Lines and Waveguides" organized by CEG Anna University, INDIA from 24-May-2010 to 30-May-2010.

10. Participated in a International level workshop on "workshop on eContent Development skills for Teachers" organized by CEG Anna University, INDIA from 15-Sep-2010.

11. Participated in a International level conference on "24th international conference on VLSI design" organized by VLSI Society of India, INDIA from 02-Jan-2011 to 07-Jan-2011.

12. Participated in a International level conference on "PhD Research in Micro Electronics" organized by IEEE Circuits and Systems, Italy from 03-Jul-2011 to 07-Jul-2011.

13. Attended a International level Short Course on "FDP on EC2401- Wireless Communication" organized by CEG, Anna University, INDIA from 20-May-2012 to 26-May-2012.

14. Participated in a International level workshop on "workshop on PLL Theory & Design" organized by VLSI Society of India, Cadence, Analog Devices, INDIA from 06-Dec-2012 to 08-Nov-2018.

15. Participated in a International level workshop on "Workshop on High Speed PCB Design from Front End to Back End Using Allegro" organized by NIEIT, Chennai, INDIA from 03-Oct-2013 to 04-Oct-2014.

16. Participated in a International level conference on "International Conference on Circuits,Communication, Control and Computing 14C2014" organized by M.S. Ramaiah Institute of Technology, Bangalore, INDIA from 21-Nov-2014 to 22-Nov-2014.

17. Participated in a International level conference on "1 st International Conference on Nano -electronics, Circuits and Communication Systems" organized by IETE &ISVE Ranchi, INDIA from 09-May-2015 to 10-May-2015.

18. Attended a International level Short Course on "Millimeter -Wave Integrated Circuits:60GHz and Beyond, GIAN Course" organized by GIAN IITM, INDIA from 01-Jan-2016 to 17-Jan-2016.

19. Participated in a National level workshop on "Training Programme on Change management &capacity building to improve quality of service" organized by CEG, Anna University, INDIA from 23-Feb-2016.

20. Attended a International level Short Course on "Fundamentals of Numerical Modelling and Simulation of Multi-Physics," organized by GIAN IITM, INDIA from 30-Jan-2017 to 03-Feb-2017.

21. Attended a International level Short Course on "Computational Techniques for Frequency domain and Perturbation Analysis of Electronics and Multi-Physics Systems" organized by GIAN IITM, INDIA from 13-Mar-2017 to 18-Mar-2017.

22. Attended a International level Short Course on "FDP on Advanced Digital signal Processing" organized by CEG, Anna University, INDIA from 24-May-2018 to 30-May-2008.

Experience Abroad

1. Visited IEEE Circuits and Systems Society, Italy from 03-Jul-2011 to 07-Jul-2011. Purpose of visit :Presentation and Participation.

Invited Lectures

1. Delivered a Lecture on "Design and testing Sequential Circuits" in National level Workshop on Advances in VLSI Circuit Design using XILINX organized by Pondicherry University, Pondicherry (22-Aug-2014).

Extension & Outreach Programme

1. Course Instructor, BSc Electronics honors practical, participated by Online Course and funded by UGC and EMMRC Anna University at EMMRC Anna University during 31-Dec-1969 and 31-Dec-1969. No. of participants: 0.